What is claimed is:

1. A nonvolatile semiconductor memory device comprising a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction,

wherein each of the memory cells includes a source region, a drain region, a channel region between the source region and the drain region, a word gate and a select gate disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region,

wherein the memory cell array includes:

a plurality of wordlines, each of the wordlines being connected in common with the word gates of the memory cells arranged in the row direction;

a plurality of selectlines, each of the selectlines being connected in common with the select gates of the memory cells arranged in the row direction;

a plurality of bitlines, each of the bitlines being connected in common with the drain regions or the source regions of the memory cells arranged in the column direction;

a wordline-and-selectline driver section which drives the wordlines and the selectlines; and

a bitline driver section which drives the bitlines,

wherein the wordline-and-selectline-driver-section includes a plurality of unit wordline-and-selectline-driver-sections, and

wherein each of the unit wordline-and-selectline driver sections drives the select gates and the word gates of the memory cells in each row at a single potential.

2. The nonvolatile semiconductor memory device as defined in claim 1,

wherein a wordline among the wordlines and a selectline among the selectlines

are short-circuited, the wordline and the selectline being connected with the same memory cells.

3. The nonvolatile semiconductor memory device as defined in claim 2,

wherein an interconnect contact is provided over the wordline and the select line, and

wherein the interconnect contact covers a part of an interconnect surface of the wordline and a part of an interconnect surface of the selectline.

4. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the word gate and the select gate are capacitively coupled in each of the memory cells.

5. The nonvolatile semiconductor memory device as defined in claim 4,

wherein the wordline-and-selectline-driver-section supplies drive voltages to the wordlines or the selectlines connected with the memory cells.

6. The nonvolatile semiconductor memory device as defined in claim 4,

wherein each of the unit wordline-and-selectline-driver-sections supplies drive voltages to a wordline among the wordlines or a selectline among the selectlines connected with the same memory cells.

7. The nonvolatile semiconductor memory device as defined in claim 4,

wherein the nonvolatile memory element is formed to extend between the word gate and the select gate of each of the memory cells.

8. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the nonvolatile memory element is formed of an ONO film which includes two oxide films (O) and a nitride film (N) between the two oxide films (O).

9. The nonvolatile semiconductor memory device as defined in claim 1,

wherein each of the memory cells includes a first region and a second region in the channel region, the first region being adjacent to the source region, and the second region being adjacent to the drain region, and

wherein the select gate is disposed over the first region, and the word gate is disposed over the second region with the nonvolatile memory element interposed in between.

10. The nonvolatile semiconductor memory device as defined in claim 1,

wherein each of the memory cells includes a first region and a second region in the channel region, the first region being adjacent to the source region, and the second region being adjacent to the drain region, and

wherein the word gate is disposed over the first region with the nonvolatile memory element interposed in between, and the select gate is disposed over the second region.